國 立 臺 北 科 技 大 學

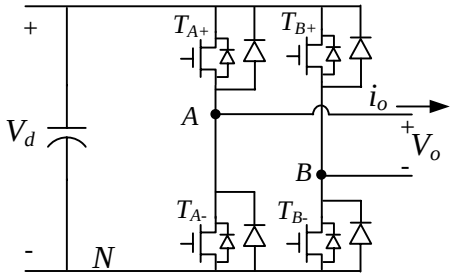
九十七學年第一學期電機系博士班資格考試

電力電子電路分析與設計試題

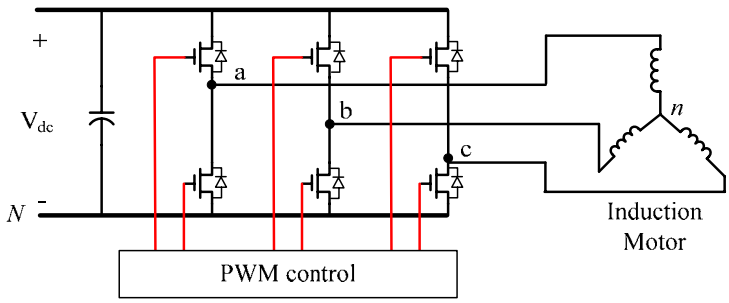
注意事項：

1. 本試題共【5】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。
4. 考試時間:二小時。**(可以使用計算機)**

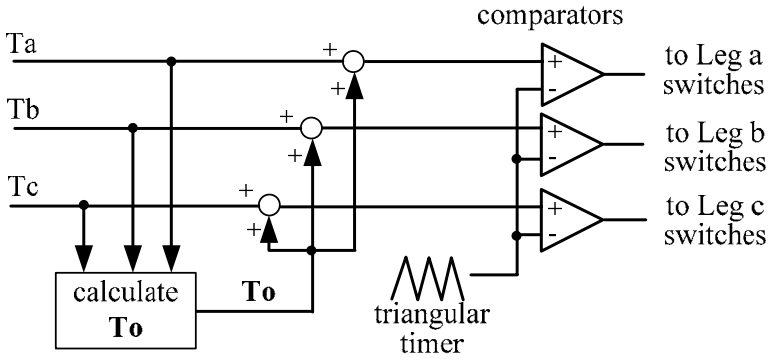
1. (*20%*) Consider the single-phase full bridge DC-AC inverter shown below. In general, following PWM modulation strategies are implemented: (a) **unipolar voltage switching**, (b) **even frequency modulation ratio** is selected. Explain the advantages of using these PWM strategies for single phase DC-AC inverter?



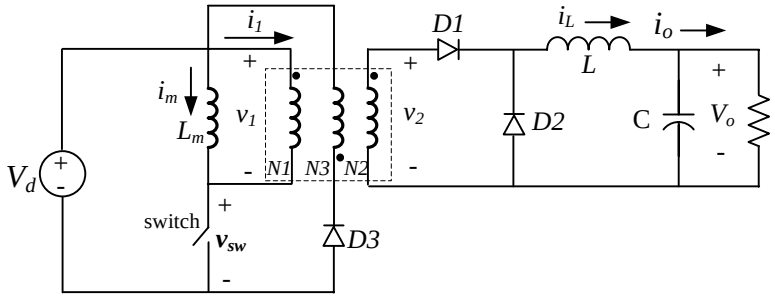
2. (*20%*) Following circuit shows a three-phase DC-AC Inverter for induction motors. If the motor is modulated with **Sinusoidal PWM** (SPWM), V_{dc} is the bus voltage. Then, what is the maximum fundamental motor phase voltage attainable with SPWM without over-modulation? Why?



3. (*20%*)　In general, **Space-Vector PWM** (SVPWM) modulation strategy for three-phase DC-AC inverters can be implemented with harmonic injections. A schematic of the harmonic injection PWM using timer signals is shown in the following figure, where Ta, Tb, and Tc are the timer signals for phase A, B, and C, respectively, and **To** represents the harmonic signal injected. The basic idea is to move the **non-zero voltage region** to the center of the switching period. If the timer varies from 0 to 4095 (i.e. period Ts = 4096), and for a certain instant, Ta = 4065, Tb = 731, and Tc = 1348. Find **To** at this instant?



4. (*20%*) Following circuit shows a forward converter. The isolation transformer has three windings and already been replaced with its equivalent circuit in the circuit. The leakage inductances of the transformer are neglected and the mutual inductance is L_m. If $\boldsymbol{V_o}$ is fixed, duty of the switch is $\boldsymbol{D}$, find the relationship between $\boldsymbol{I_o}$, $\boldsymbol{V_d}$, and $\boldsymbol{D}$ when the converter is operating on the boundary between **continuous** and **discontinuous** conduction mode?



5. (*20%*) Design a driver circuit for a DC-AC inverter leg (upper and lower switches) using power MOSFETs. The Switches are denoted as S_1 and S_2, respectively, and assuming that there can be turned on/off with 15V and 0V. The input logic signals (+5V) are CS_1 and CS_2, they control S_1 and S_2, respectively. S_1 (S_2) is turned on when CS_1 (CS_2) = 5V, and turned off when CS_1 (CS_2) = 0V. In the driver circuit, the input signals should be isolated from the power stage. Two sets of 15V isolated power supplies are available for signal isolations. Note that the reference point of $15Vi_2$ is tied to the negative bus. The isolation can be accomplished with opto-couplers, its symbol is shown in the following figure. Draw the circuit with the schematics of the actual components. Use any components in the circuit should it be necessary, for example resistors, capacitors, and logic buffers. You can assume that all the components are properly rated.