## 國立臺北科技大學 九十六學年第二學期電機系博士班資格考試

## 高等類比積體電路設計試題

填學生證號碼

第一頁 共九頁

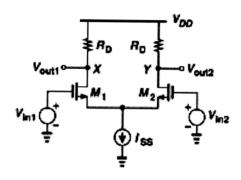
## 注意事項:

- 1. 本試題共【8】題,配分共100分。
- 2. 請按順序標明題號作答,不必抄題。
- 3. 全部答案均須答在試卷答案欄內,否則不予計分。
- 4. 考試時間:二小時。

1. (10%) (a) What is the channel-length modulation effect? (b) What is the body effect?

2. (10%) Sketch the circuit and layout of CMOS source follower.

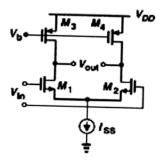
3. (10%) According to the following figure, find the differential-mode gain ( $|A_{DM}|$ ), common-mode gain ( $A_{CM-DM}$ ) and CMRR, respectively, if the output impedance of current source  $I_{SS}$  is infinity and all of the components are matched.



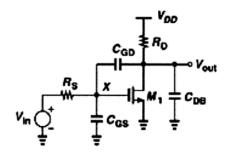
4. (15%) In the following figure, please find the three poles of this amplifier using Miller effect.

 $V_{DO}$   $R_{D}$   $V_{Out}$   $V_{DO}$   $V_{DO}$   $V_{Out}$   $V_{OB2} + C_{DB2} + C_{L}$   $V_{ID}$   $V_{ID}$ 

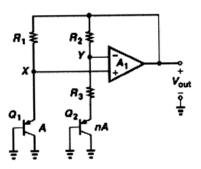
5. (10%) In the following figure, the voltage  $V_b$  is the bias voltage, please find the small-signal differential gain  $V_{out}/V_{in}$ .



6. (10%) In the following figure, use Miller effect to find the two poles and one zero, respectively.



7. (15%) Please find the output voltage  $V_{out}$ , as shown in the following figure. If  $V_{out}$  will be a reference voltage and independent to temperature, please find the condition.



8. (20%) According to the following figure, find closed-loop input resistance ( $R_{i,closed}$ ), closed-loop output resistance ( $R_{o,closed}$ ) and closed-loop gain ( $A_{i,closed}$ ), respectively.

