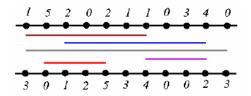
## 國立臺北科技大學

## 一百零三學年第二學期電機系博士班資格考試

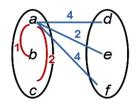
## 積體電路實體設計演算法 試題



- 本試題共【8】題,配分共100分。
  請按順序標明題號作答,不必抄題。
  全部答案均須答在試卷答案欄內,否則不予計分。
- 1. (a) Give an example of "hypergraph". (5%)
  - (b) What does "relaxation" mean when finding the shortest path of a DAG? (5%)
  - (c) What does  $e^{\frac{-\Delta c}{T}}$  mean in Simulated Annealing algorithm? (5%)
  - (d) For the following routing problem, draw its Horizontal Constraint Graph (HCG). (5%)



- 2. Based on KL partitioning algorithm,
  - (a) For the connection as shown below, what is the D-value of vertex a? (5%)
  - (b) Why is KL algorithm a "balanced" partitioning heuristic? (5%)



- 3. Elmore model has been widely used in the field of physical design.
  - (a) What is this model used to evaluate? (5%)
  - (b) Briefly describe the principle of Elmore model. (5%)
- 4. Design CMOS logic gates for the function F = (A+BC)'. (10%)
- 5. A typical formula for calculating cost function of a floorplan is shown below, what does A, λ, and W respectively mean? (10%)

6. Express the following floorplan in slicing tree and Polish expression respectively. (10%)



- 7. Given the following Polish expression E = 12H3V45HH6V,
  - (a) Does the above expression satisfy the balloting property? Justify your answer. (5%)
  - (b) Is E a normalized Polish expression? If not, change an operator and its adjacent operand to transform E into a normalized Polish expression E. (5%)
- 8. (a) Describe the principle of Lee's algorithm (or maze routing). (10%)
  - (b) Label the grids after performing Lee's algorithm on a  $5\times5$  grids with an obstacle (colored black), where the start grid (S) and target grid (T) are respectively located at (4, 4) and (0, 1). (10%)

