國 立 臺 北 科 技 大 學

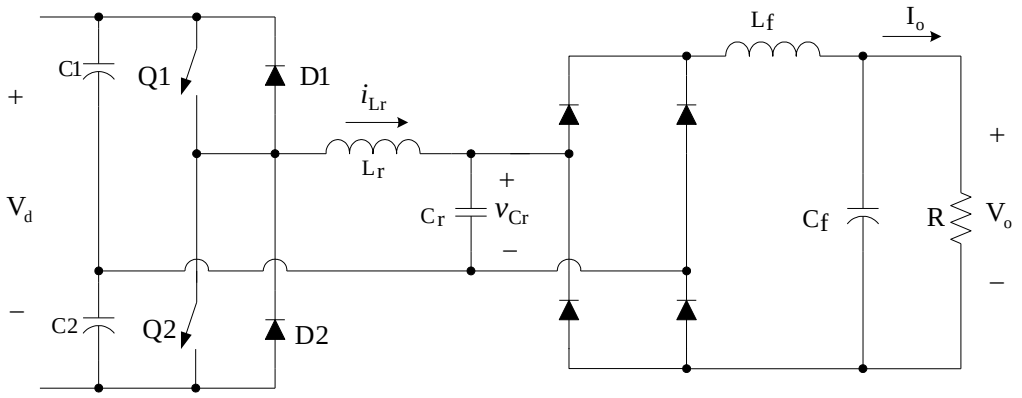
九十九學年第二學期電機系博士班資格考試

切換式電源設計 試題

注意事項：

1. 本試題共【4】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。
4. 考試時間:二小時。

1. A parallel resonant converter is shown as below. Please illustrate the operations for each time-duration in case of $f_s > f_0$, where f_s is the switching frequency and f_0 is the resonant frequency, including the equivalent circuits, the resonant equations depicting each equivalent circuit state and the waveforms on C_r and L_r. While the input voltage V_d=100V, the resonant capacitor C_r=0.32μF, the resonant inductor L_r=8μH, the output current R=10Ω and the switching frequency f_s=120kHz depending on the above analysis, please determine the output voltage.　35%



2. Please explain operation of a RCD turn-off snubber and design one used in Forward converter for the output power P_o=150W, the input voltage V_d=160V ranged from 136V to 184V, the duty cycle D_{max}=0.4 corresponding to the minimum input voltage, the switching frequency f_s=100kHz and the efficiency η=0.8 wherein the peak current just before turnoff is assumed as the peak flat-topped value, the used transistor current fall time is 0.3μs and the minimum turn-on time is 3μs (because maximum and minimum input voltages are 15 percent above and below the nominal value, 4μs/1.3=3μs). 20%

3. A boost is used to supply a load current of 1A from a voltage source having a range of 27V~42V. A known control circuit is used to regulate the output voltage at 80V by modulating the duty cycle and the switching frequency is selected as 200kHz. Please design the storage inductance such that the variation in the inductor current is no more than 40 percent of the average inductor current for all operating conditions and determine an ideal capacitance such that the output voltage ripple is no more than 2 percent. In terms of a non-ideal capacitor having the equivalent series resistance (ESR), please determine the maximum ESR for a 2-percent ripple. 25%

4. In one converter operating from a nominal 115-Vac line with ±10% tolerance, MOSFET is used, given that the Cgs=1800pF and Cgd=150pF, and the gate is driven up to 10V “on” level in a rise time 50ns. Please calculate the total current required from the gate driving source. 20%